# VIDEO CAMERA WITH FPGA COMPUTATIONAL UNIT

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**Abstract**: This paper describes a framework for integration of image/video pre-processing functionality into a video camera that includes programmable hardware (FPGA). The purpose of the paper is to demonstrate the feasibility of the idea of integrating functional blocks into video cameras, to show a simple method of including the pre-processed results into video camera image data, to demonstrate applications that can benefit from pre-processing, and to present the functional example of the camera with simple functional block along with discussion of the results and conclusions.

**Keywords**: Image/video pre-processing, FPGA

## 1 INTRODUCTION

Video camera technology and computer technology is often used in applications where the image/video is processed in a computer in order to extract important information. The demand for complexity of algorithms as well as the demand for small size of embedded systems with low power consumption, etc. is increasing. At the same time, programmable hardware is becoming an important part of video camera design and design of electronic circuits attached to the cameras. Therefore, the possibility of exploring a potential including some pre-processing functionality in a programmable hardware attached to the video camera becomes interesting and this paper presents results of exploration of a possible way how to implement such a functional device.

In this paper, the feasibility of the idea of integrating functional blocks into video cameras is demonstrated and approach is proposed. The approach says that is possible to integrate some computational blocks into video camera so that the captured images are pre-processed inside the video camera and pre-processed images are sent to the camera output so that the following software image processing is easier. However, in general it is a problem how to easily transfer pre-processed image data to image processing software. This problem is solved and described in this paper too. In case of implementation of the pre-processing unit to the camera that already includes programmable hardware, it means that the camera contains an image/video stream interface that can be used for purposes of proposed concept.

R.Mosqueron, J.Dubois and M.Paindavoine [1] describe implementation of two image processing algorithms in FPGA embedded inside the camera. S.McBader and P.Lee [2] present parallel programmable architecture for signal pre-processing implemented in FPGA. Seung Hun Jin, Jung Uk Cho and Jae Wook Jeon [3] propose pipelined virtual camera configuration for real-time image processing based on FPGA. S.H. Hajimowlana, G.A. Jullien, R. Muscedere and J.W.Roberts [4] describe a prototype system for developing real-time video-rate data stream processing algorithms for automated machine vision systems. Hyun Lim, Soon-Young Park, Seong-Jun Kang and Wan-Hyun Cho [5]present an FPGA implementation of a watermarking-based authentication algorithm for a digital camera to authenticate the snapshots in a manner that any changes of contents in the still image will be reflected in the embedded watermark.

This paper is organized as follow. The proposed processing unit system integration is described in Section 2. The studied computational unit is introduced in Section 3. Results of implementation is described in Section 4. Finally, conclusions and future worked are drawn in Section 5.

## 2 COMPUTATIONAL UNIT SYSTEM INTEGRATION

Figure 1 shows typical image processing path. Figure 1 shows typical image processing path. Input

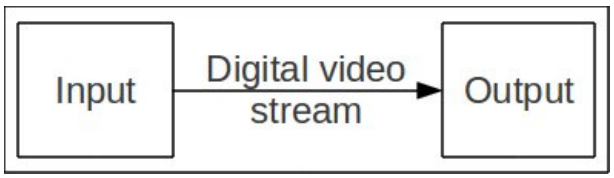


**Figure 1:** Block scheme of general camera

block contains all the camera units that are necessary to create a digital video stream. The input block can contain for example CCD sensor and A/D converter. The output block presents the units needed to export the acquired data from camera to the outside world. For example, there might be some compression units, USB interface, etc. Digital data stream is the right place for the computational unit integration as shown in Figure 1. Computational unit has limits that are caused by its integration

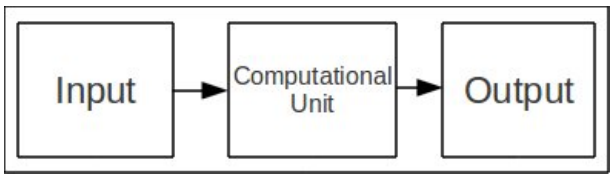


**Figure 2:** Block scheme of general camera with computational unit.

into video data stream. Moreover, the output has to be in the same format as the input. Products of computations in computational unit have to be integrated into video data stream without changes of video data stream format. Consequently, all products of computational unit have to be possible to present in video data stream.

Let's assume that a camera exists, where the image data flows throw a programmable chip. It can be solution from Xilinx with FPGA [6] , solution from Xilinx with DSP [7], solution from Camea UnicamD2 [9] with FPGA, solution from Texas Instruments [8] with DSP or any other.

## 3 COMPUTATIONAL UNIT

This section describes integration and interface of computational unit, whlie the functionality and parameters of unit are not discussed. The functional unit included in the electronics of video camera, as mentioned earlier in this paper, was originally intended as a pre-processing unit for embedded systems, but its exploitation can be wider, e.g. in:

- Incorporating the output of processing into a human observer suitable visible information. The algorithms suitable in this case may include changing the original image into a filtered one, inclusion of some statistical information about the image into the image in a text form, visualizing some image features, such as histogram, etc.
- Incorporating the output of pre-processing into the image but in a form not necessarily directly usable for human observers in order to relieve that attached computer, e.g. to enable implemen-

tation of some applications on embedded systems with limited computational capabilities or to enable processing input from multiple (many) cameras in high performance computer system. The algorithms to be implemented in this case may include:

- median value in a region in order to support efficient dynamic thresholding,
- general image filtering (linear and non-linear),
- histogram processing for multiple threshold applications,
- object detection using AdaBoost or similar methods,
- image imperfections corrections, such as reduction of noise,
- high dynamic range video conversion, etc

The computational unit acquires image data on its input and sends pre-processed image to its output. The pre-processed information has to be sent to a camera output. This template shows our way of transfer this data. Some part of image should be used as a carrier of data. We are solving only digital data transfer, because analog data transferring is problem because its vulnerability to data lost. Computational unit creates new data, that can be appended to image as shown in Figure 3.


**Figure 3:** Adding data to an image

Computational unit interface is shown in Figure 4. Interface contains 8 bit data vector and control signals Frame, Line and CLK. Frame signal defines time window when the 8bit data vector represents an image. Line signal defines valid line, which is time window when 8 bit data represents one complete line. The last signal of this interface is CLK. Data vector and control signals are synchronized by clock signal. Rows are corresponding with CLK.

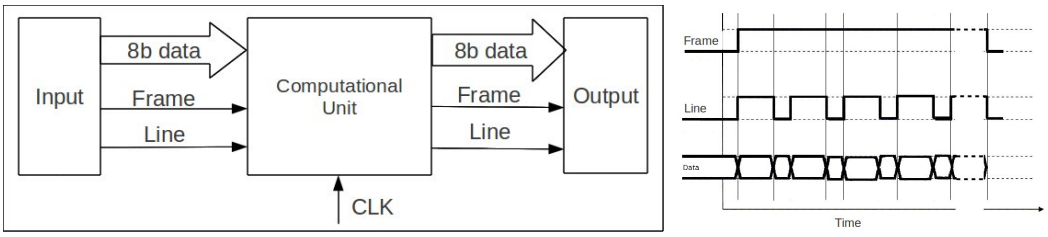


**Figure 4:** Interface of computational unit

## 4 EXPERIMENTS AND RESULTS

For this project, we have used a digital camera CAMEA UnicamD2[9]. Camea UnicamD2 shown in Figure 5 contains Xilinx Spartan-3 XC3S400 FPGA. This camera was created especially for using in Unicam traffic monitoring systems [9] as a speed control, red light violation detection, stolen or wanted vehicle search etc.The proposed principle was demonstrated by implementation of a dummy unit and a simple unit that modifies the data. An example of modified image from video stream is shown in Figure 6. In this case, new data (in red box) was added to the right end of the image as was shown in Section 3. Utilization of this FPGA and estimation of utilization bigger Xilinx Spartan-3 XC3S1000 FPGA is in Table 1. Utilizing of FPGA is high because the FPGA contains all the

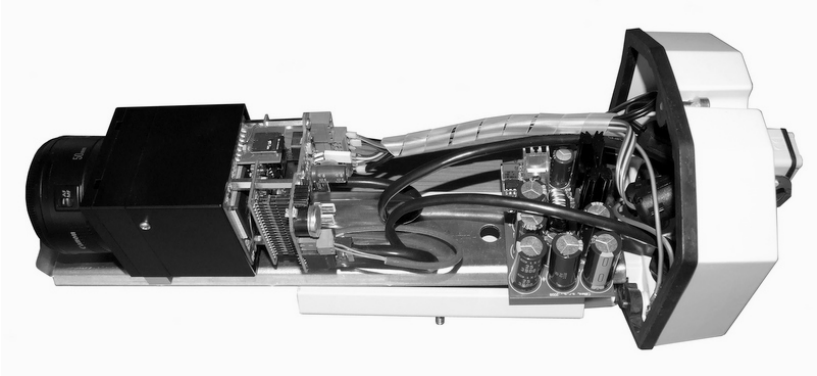

**Figure 5:** Photo of Camea UnicamD2

**Figure 6:** Adding data to a real image

video data stream manipulation units. Table 1 shows estimated utilization of bigger Xilinx Spartan-3 XC3S1000 FPGA that could be used instead of Xilinx Spartan-3 XC3S1000 FPGA .

**Table 1:** Xilinx Spartan-3 XC3S400 Utilization Summary

| blocks | used | capacity | utilization | XC3S1000 estimation |
|---|---|---|---|---|
| BUFGMUXs | 6 | 8 | 75% | 40% |
| DCMs | 2 | 4 | 50% | 30% |
| External IOBs | 78 | 141 | 55% | 38% |
| LOCed IOBs | 78 | 78 | 100% | 68% |
| RAMB16s | 13 | 16 | 81% | 56% |
| LOCed RAMB16s | 11 | 13 | 84% | 58% |
| Slices | 2798 | 3584 | 78% | 54% |
| SLICEMs | 11 | 1792 | 1% | 1% |

## 5 CONCLUSIONS

The presented paper demonstrated a proof of concept of video camera with FPGA hardware with built-in functional unit for image/video pre-processing. The video camera hardware has been described and the sample processing unit built in the camera has been demonstrated. The experiments showed that the consumption of resources is dependent on implemented algorithm. Easy units are very small, but the implementation of sophisticated functional units might probably cause changing the Xilinx Spartan-3 XC3S400 FPGA for bigger type of Xilinx Spartan-3 family FPGA. The future worked includes preparation of more sophisticated functional units, such as object detection, etc., experiments to show feasibility of the video cameras with functional units in applications, and

further improvements in the functional blocks demonstrations.Table 1: Xilinx Spartan-3 XC3S400 Utilization Summaryblocks used capacity utilization XC3S1000 estimation

## ACKNOWLEDGEMENT

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